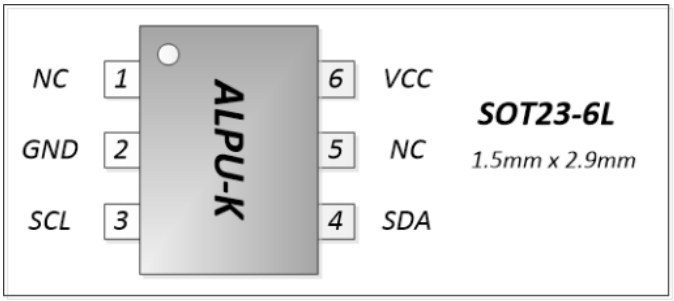
Features

- User programmable copy protection IC
- 4,096-bit MTP, Retention: 10 years, Erase/Write Endurance: 10K
- Standard AES-256 encryption and decryption
- I^2C Serial Interface, Supporting up to 400 kbps
- Two User Zone Area, UserZone Key, User-Serial, Monotonic Increase Memory, eFuse
- Built- in Power on Reset / 6.7MHz OSC
- Two Power Mode (Active, Sleep)

Applications

- Print cartridge, Beauty device
- IoT edge Device, IP Camera, CCTV
- Set-Top Boxes
- Walkie-talkie, ADAS

Pin Configuration



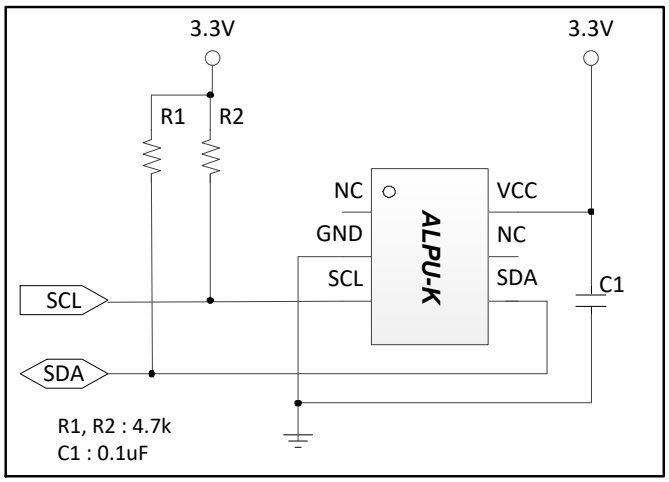
Ordering Information

Part	Operation Voltage	Package Type
ALPU-K	3.3V	SOT-23-6L

General Description

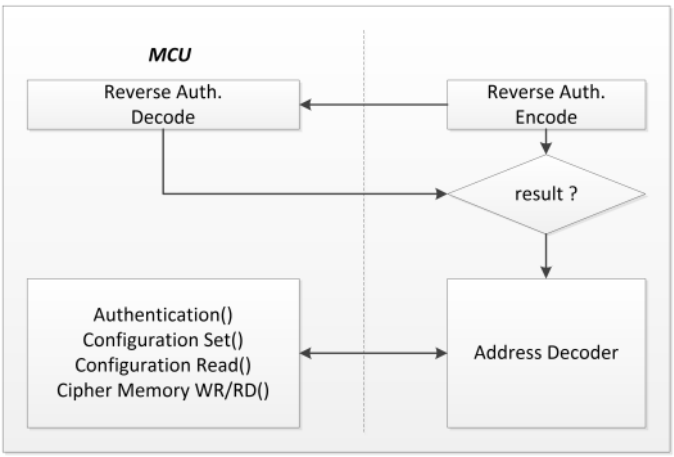
The **ALPU-K** is the **highest-performance IC** in the ALPU series, featuring an encryption core based on the **AES-256 algorithm** and an internal **4-Kbit non-volatile memory**. It interfaces seamlessly with a host MCU via a serial bus.

Typical Operation Circuit



< SOT-23-6L Package Type >

Encryption Flow



1 Features

Security

- High performance illegal copy protection IC
- AES-256 cipher memory write/read
- Two userZone, each with its own key

Memory

- 4,096-bit MTP memory
- 32-bit user serial
- Monotonic Increase Memory (1 ~ 10,000)
- eFuse UserZone, eFuse UserConfig

  Not writable when eFuse is enabled

  User Zone, User Zone Key, User Serial

Peripheral

- I²C serial interface, Support up to 400 kbps
- Built in LDO (Low Drop Voltage)
- Built in OSC (6.7 MHz)
- Built in POR (Power-On-Reset)
- Two Power Modes: Active, Sleep

3.3 V Operation voltage

- Core Voltage 1.1 V

SOT23 6L Package

1.1 Block Diagram

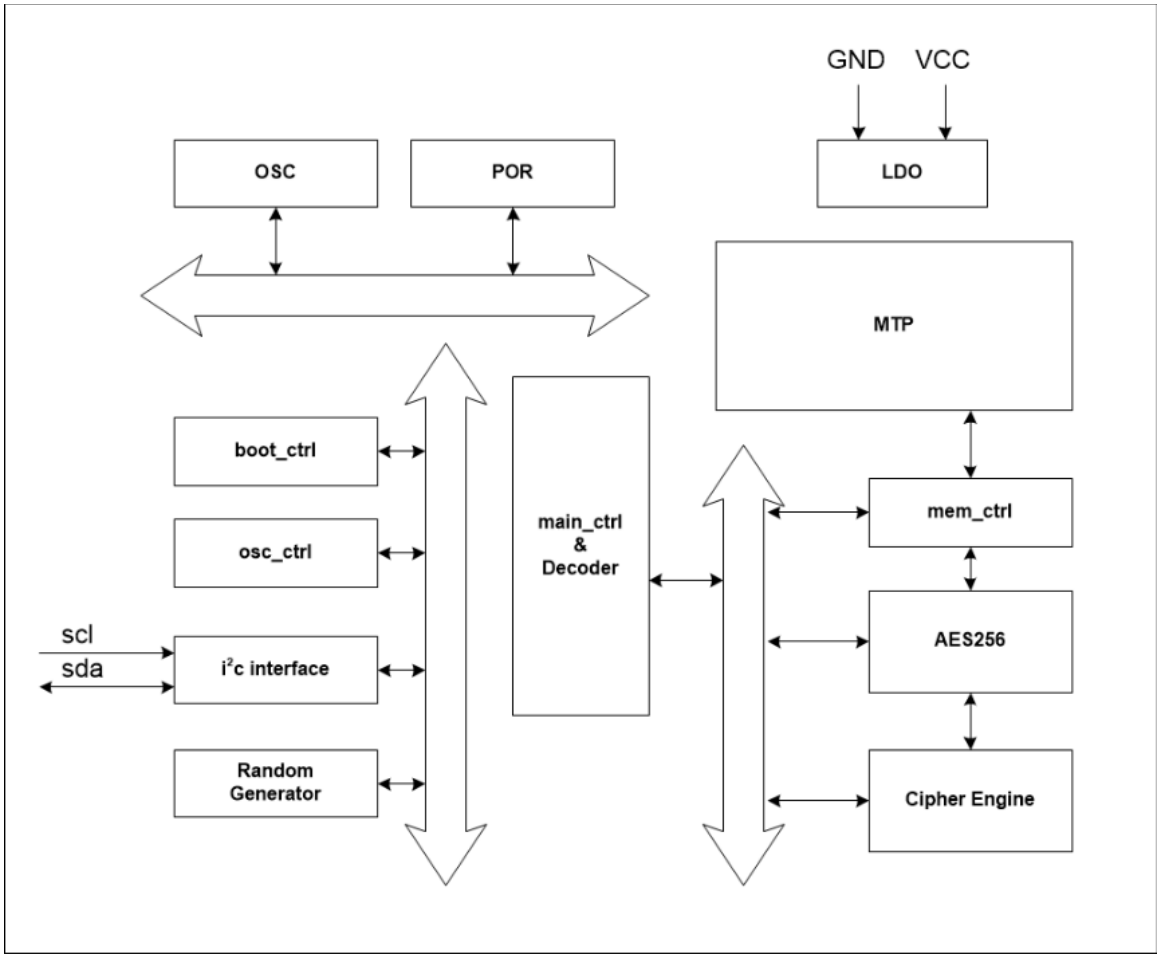


Figure 1-1 Block Diagram

1.2 Pin Configurations

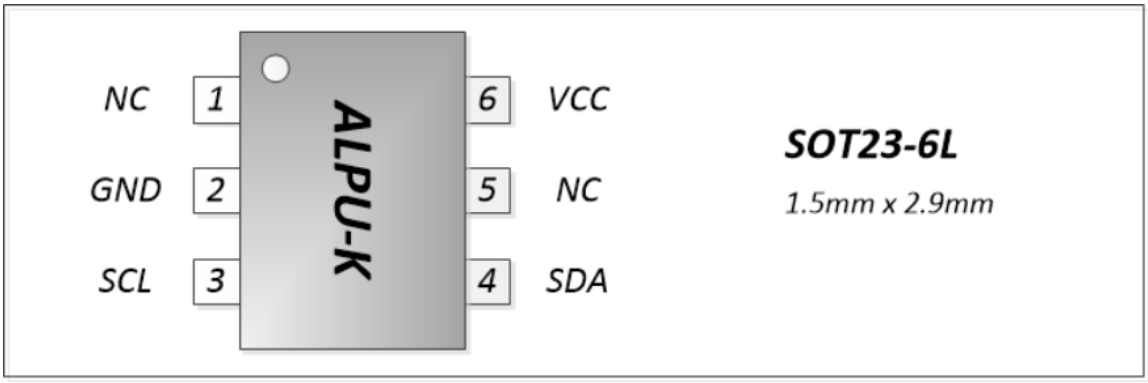


Figure 1-2 pin configurations

1.3 Pin Description

Table 1-1 Pin Description

Pin Num	Pin Name	Description
1	NC	Not Connect
2	GND	Ground
3	SCL	I²C Serial Clock input pin. CMOS Input
4	SDA	I²C Serial Data, CMOS Input / Open-Drain Output bi-directional I/O
5	NC	Not Connect
6	VCC	Digital supply voltage

2 I/O Port

2.1 ESD protection circuit

ESD protection circuit for the whole chip is achieved as shown in Figure2-1. It can be protected against two widely used industry standard ESD test models: Human Body Model (HBM) and Machine Model (MM). Both models test each pin against every other pin and/or a power/ground supply using a positive and a negative pulse.

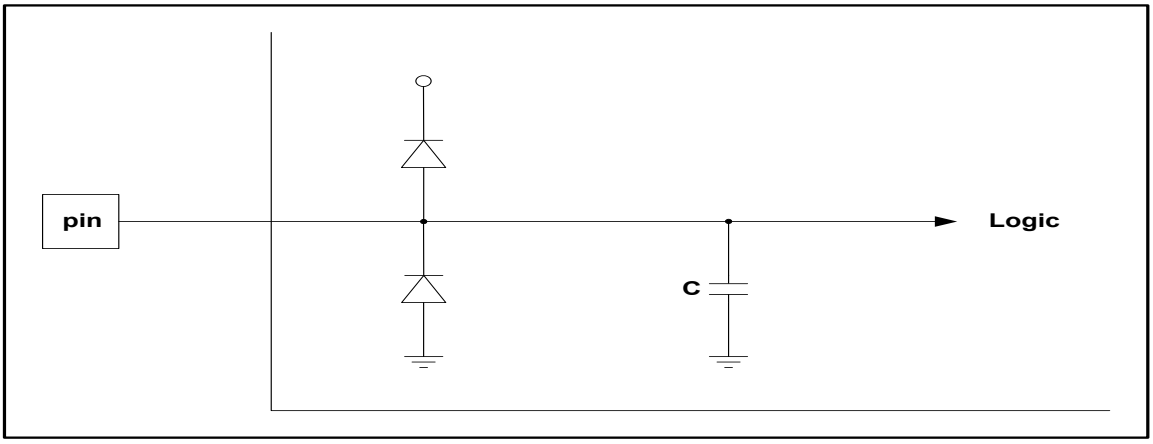


Figure 2-1 ESD protection circuit

2.2 I/O Type

ALPU-K has I/O types as shown in Table 2-1

Table 2-1 I/O Type

Direction	Name	Description
Power	VCC	Digital supply voltage
	GND	Ground
Bi-direction Port	SDA	I²C Serial Data bi-direction pin
Input Port	SCL	I²C Serial Clock input pin

Input port (SCL)

The input cell is an input buffer with CMOS input.

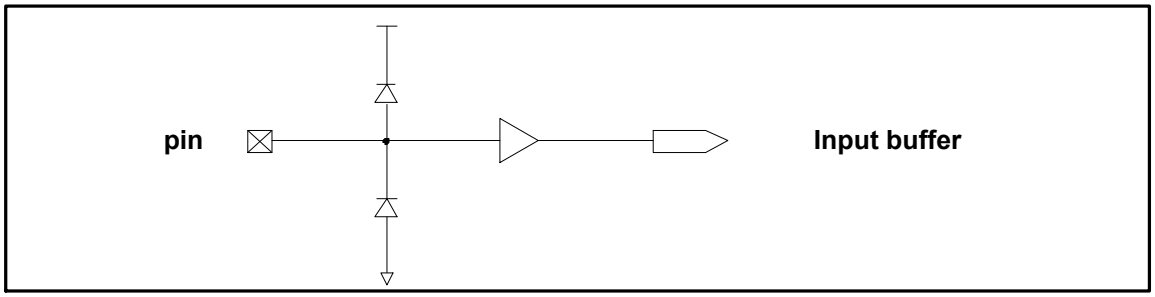


Figure 2-2 input port

Bi-direction port (SDA)

This cell is a bi-direction buffer with CMOS input and 2mA n-channel open drain output.

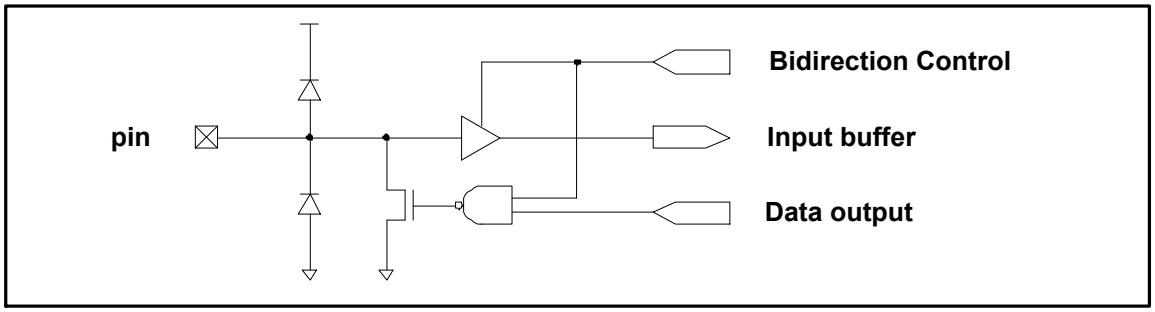


Figure 2-3 bi-direction

3 Clock Management

3.1 Internal clock

All inner blocks use internal OSC. Internal OSC is approximately 6.7MHz shown in Table 3-1.

Table 3-1 Internal clock

PARAMETER	SYMBOL	CONDITION	Min	Typ	Max	Unit
Frequency			6.1	6.7	6.4	MHz
Frequency Variation	Δf67m	-40 ≤ Ta ≤ 80°C	-	-	±10	%
Duty Cycle	Dmax		48	50	52	%

3.2 Clock On/Off

Internal OSC clock can be turned on or off. If ALPU-K is in the condition of Sleep-mode, then internal OSC clock is turned off to save the power. Here is the condition to enter the Sleep-mode. SCL and SDA pins both stay high and all functions are disabled for more than 2 seconds. The OSC wakes up from Sleep-mode and turns the clock on only when the I²C device-address correct.

4 Power Mode

ALPU-K supports the power saving mode called Sleep-mode in which internal oscillator is off.

4.1 Condition of entering sleep-mode

Here is the condition to enter the Sleep-mode. SCL and SDA pins both stay high and all functions are disabled for more than 2 seconds. (Refer to Figure 4-1)

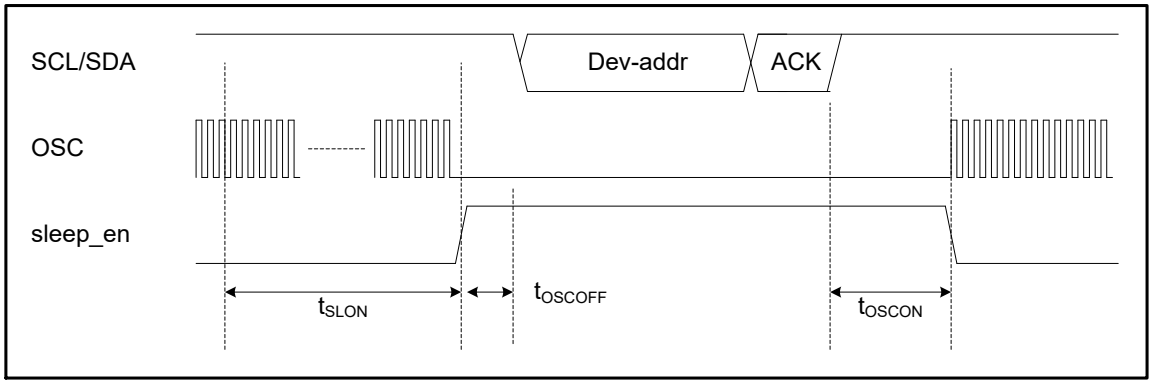


Figure 4-1 Sleep mode

- SCL/SDA: I²C signal
- sleep_en: internal signal(Oscillator On/Off signal)
- OSC: Internal oscillator (6.7 MHz)

Table 4-1 oscillator on/off timing

Parameter	Symbol	MIN	TYP	MAX	Unit
Sleep-mode On Time	t_{SLON}	2,000			ms
OSC On Time	t_{OSCON}			5	us
OSC Off Time	t_{OSCOFF}			10	ns

4.2 Condition of exiting sleep-mode

Wakeup occurs only if the I²C device-address is correct. (Refer to Figure 4-1)

5 Initialization

ALPU-K has an internal POR (Power-on-Reset) circuit. When system power turns on ALPU-K's POR resets its own system. During reset time, all internal registers of ALPU-K are configured as their initial values. After that, internal registers are set to the values in Memory.

5.1 Start-up waveform

After RESET, the ALPU-K requires $t_{INITIAL}$ to initialize all internal registers. After $t_{INITIAL}$, the ALPU-K is ready for operation.

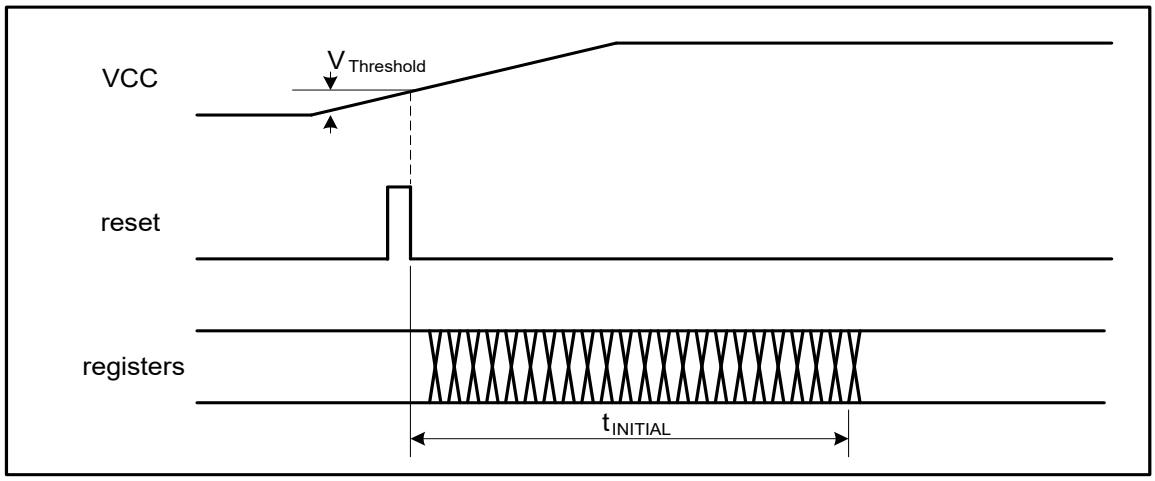


Figure 5-1 Boot initial

- VCC: 3.3V supplied power
- reset: internal POR signal
- registers: internal registers for initialization

Table 5-1 Startup timing

Parameter	Symbol	MIN	TYP	MAX	Unit
Threshold Voltage	$V_{Threshold}$	1.1	1.2	1.3	V
Initial Time	$t_{INITIAL}$			5	ms

5.2 Internal Power-On-Reset

A Power-on-Reset (POR) pulse is generated by an On-chip detection circuit. The detection level is defined in Table5-1. The POR is activated whenever VCC is below the detection level (threshold voltage). The POR circuit ensures that the device is reset from Power-on. Reaching the POR threshold voltage invokes the delay counter, which determines how long the device is kept in RESET after VCC rise.

6 Encryption

6.1 AES256 – Advanced Encryption Standard (256 bits key)

AES-256 is symmetric block cipher standardized in FIPS PUB 197. It encrypts a fixed 128-bits plaintext block under a 256 bits key through 14 transformation rounds, producing a 128 bits ciphertext block. The cipher operates on a 4x4 byte matrix called the state.

6.2 AES Block Diagram

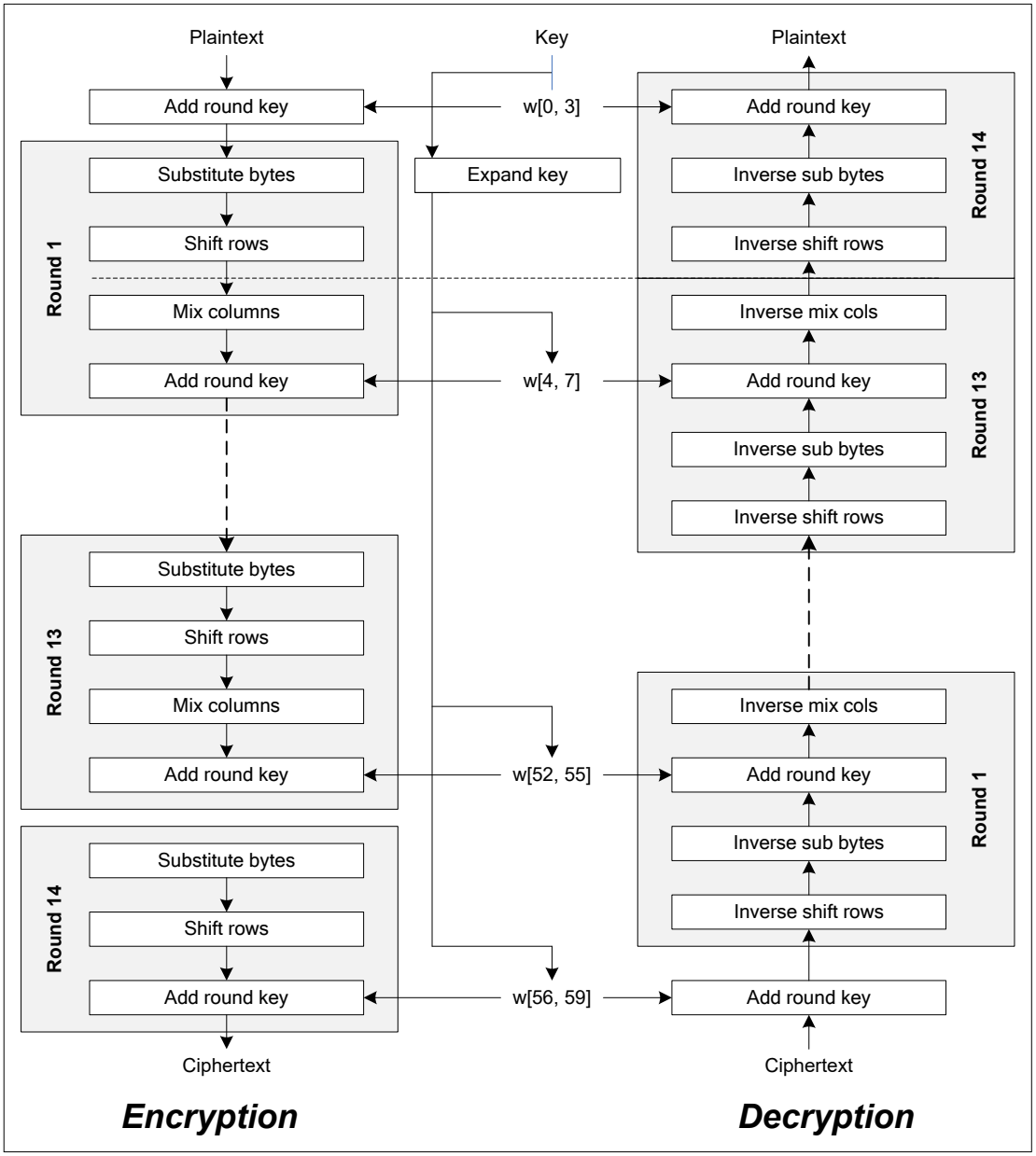


Figure 6-1 AES256 Block Diagram

- 128-bit plaintext block
- 256-bit key and key expansion process
- 14 rounds of SubBytes → ShiftRows → MixColumns → AddRoundKey
- MixColumns is excluded in the final round
- 128-bit ciphertext block as final output

6.3 Authentication flow

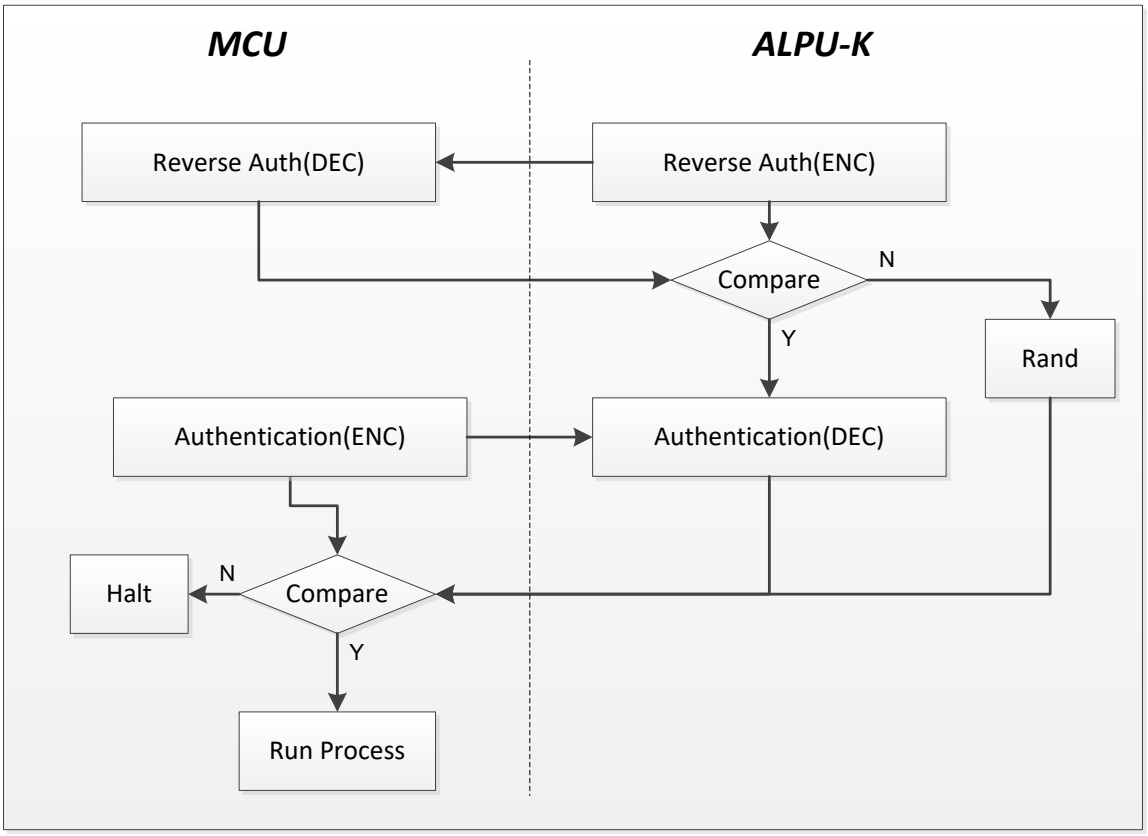


Figure 6-2 Authentication Flow

- For product authentication (activation), authentication is only possible when the reserve authentication is valid.
- Authentication is performed using the user's unique identification number.

6.4 Cipher memory flow

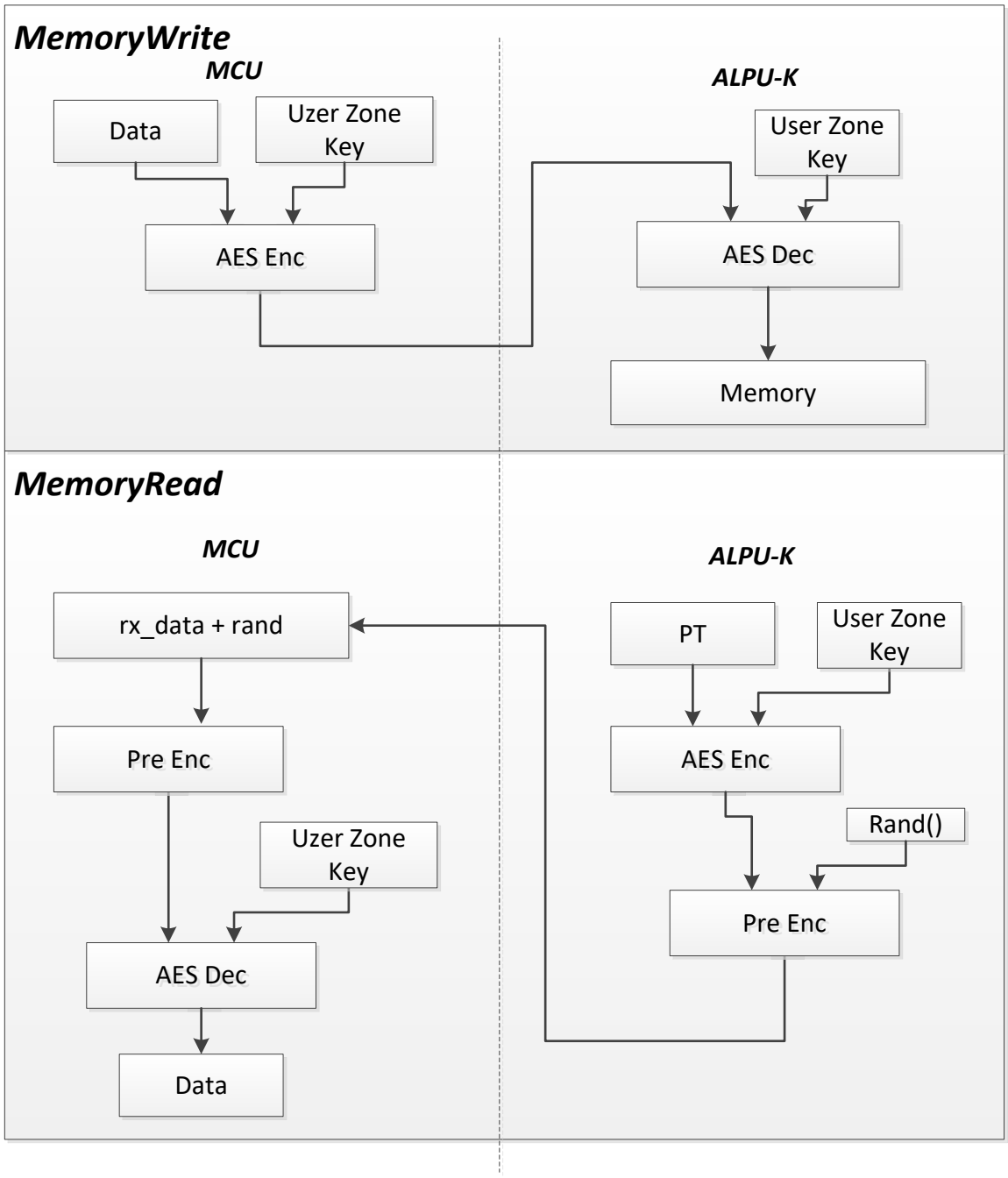


Figure 6-3 Cipher memory flow

- For memory write, the encrypted data is sent to the ALPU-K, decrypted, and then stored in memory.
- For memory reading, the data is encrypted and, using a random value, a different value is output on each read; the library then decrypts it to recover the original value.

7 Communication

7.1 I²C interface

The I²C Interface is ideally suited for typical microcontroller applications. The I²C protocol allows the systems designer to interconnect up to 128 different devices using only two bus lines, one for clock (SCL) and one for data (SDA). The only external hardware needed to implement the bus is a single pull-up resistor for each of the TWI bus lines. All devices connected to the bus have individual addresses. ALPU-K operates as a slave device on the I²C bus. I²C interface on ALPU-K is compatible with Phillips Format, supporting up to 400 Kbps

7.2 Write packet structure

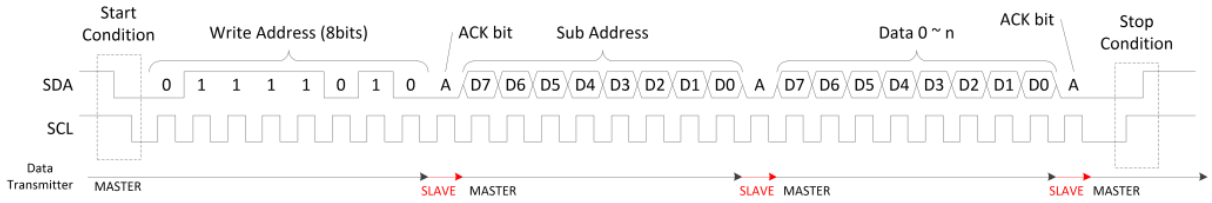


Figure 7-1 Write packet

7.3 Read packet structure

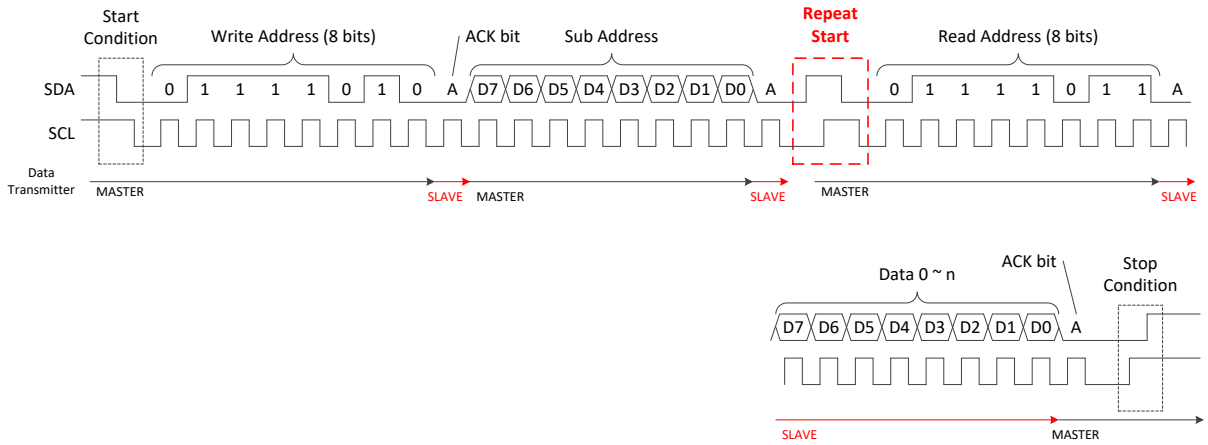


Figure 7-2 Read packet

7.4 Waveform (Start, Stop)

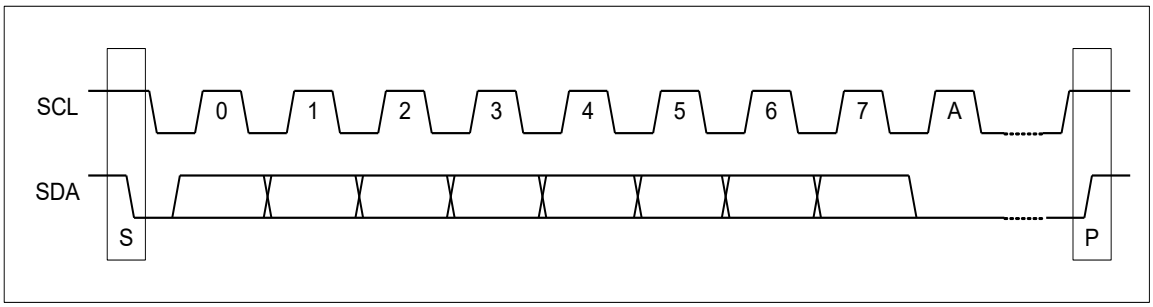


Figure 7-3 Start/stop waveform

7.5 Definition of timing

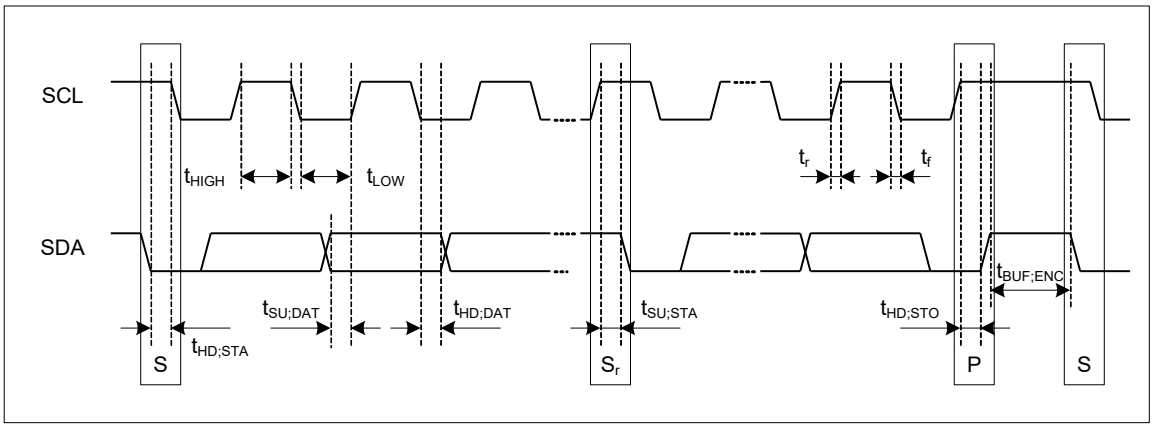


Figure 7-4 definition of I²c timing

Table 7-1 I²C timing parameters

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		MIN	MAX	MIN	MAX	
SCL clock frequency	f_{SCL}	0	100	0	400	KHz
Hold time (repeated) START condition.	$t_{HD;STA}$	4.0	-	0.6	-	us
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	us
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	us
Setup time for repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	us
Data hold time	$t_{HD;DAT}$	5.0	-	-	-	us
Data setup time	$t_{SU;DAT}$	250	-	100	-	ns
Rising time of both SDA and SCL signals	t_r	-	1000	20	300	ns
Falling time of both SDA and SCL signals	t_f	-	300	20	300	ns
Setup time of STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	us
Bus free time between STOP and START condition	$t_{BUF;ENC}^{(1)}$	1	-	1	-	ms

8 Electrical characteristics

8.1 Absolute Maximum ratings

Table 8-1 Absolute maximum ratings

Parameter	Min	Max	Units
Supply Voltage	2.7	6.0	V
Storage Temperature	-35	120	˚C
ESD Susceptibility	2000		V
DC Current VCC and GND		3	mA

Note. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied.

8.2 Recommended operating conditions

Table 8-2 Recommended operation conditions

Parameter	Min	Max	Units
Operating Temperature	-30	80	˚C
Operating Voltage	3.0	3.6	V

8.3 DC characteristics

Table 8-3 DC specifications

Symbol	Parameter	Condition	Min	Typ	Max
V_{IL}	Input Low Voltage				0.8V
V_{IH}	Input High Voltage		2.0V		
I_I	Input Leakage Current	VCC = MIN V_{IN}=GND or 3.6V			1uA
V_{OL}	Output Low Voltage	I_{OL} = 5mA			0.4V
V_{OH}	Output High Voltage	I_{OH} = 5mA	2.4V		3.6V

Table 8-4 Supply current

Symbol	Parameter	Condition	Min	Typ	Max
I_{VCC}	VCC Supply Current	Active 6.7 MHz, VCC=3.3V		2.5 mA	
		Sleep mode		200uA	

Internal IP

Table 8-5 *internal Oscillator(Ta = 25°C)*

Symbol	Parameter	Condition	Min	Typ	Max
fOSC	Switching Frequency		6.0 MHz	6.7 MHz	7.3 MHz
Δf_{OSC}	Frequency Variation	-40 ≤ Ta ≤ 80 °C	-		±10 %
Dmax	Duty Cycle		48%	50%	52%

Table 8-6 *power on reset*

Symbol	Parameter	Condition	Min	Typ	Max
Vt	Threshold Voltage		1.1 V	1.2V	1.3V
t_{RINIT}	Register Initial time				160 us

8.4 MTP Specification

DC Electrical

Table 8-7 DC Electrical

Operation Mode	parameter	MIN.	TYP.	MAX.	Unit
READ	I_{DR} (@ 1 MHz)	-	0.3	0.9	mA
WRITE	I_{DW}	-	5.5	10	mA
Standby	I_{SB}	-	1	10	uA

9 Operation Circuit

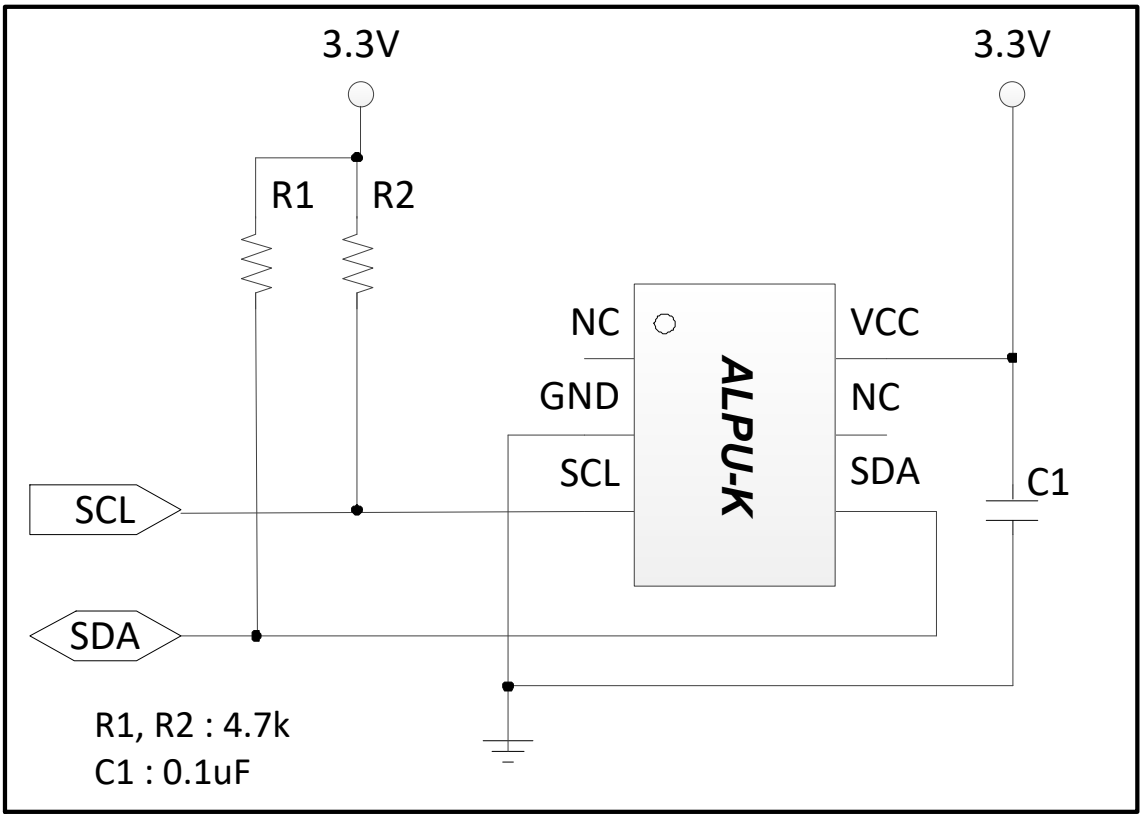
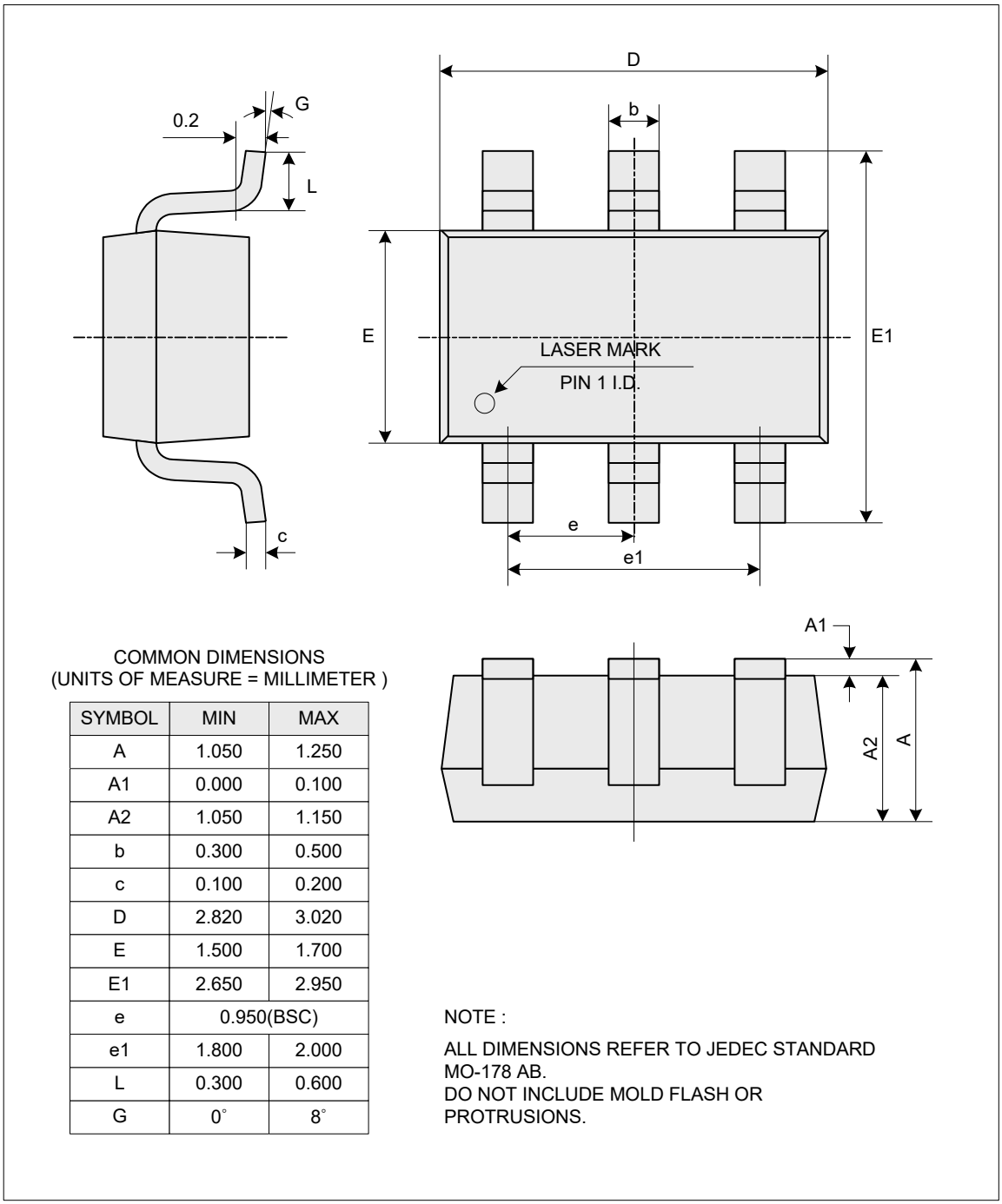


Figure 9-1 Operation circuit

10 Package Information

10.1 POD: SOT23-6L



COMMON DIMENSIONS
(UNITS OF MEASURE = MILLIMETER)

SYMBOL	MIN	MAX
A	1.050	1.250
A1	0.000	0.100
A2	1.050	1.150
b	0.300	0.500
c	0.100	0.200
D	2.820	3.020
E	1.500	1.700
E1	2.650	2.950
e	0.950(BSC)	
e1	1.800	2.000
L	0.300	0.600
G	0°	8°

NOTE :

ALL DIMENSIONS REFER TO JEDEC STANDARD MO-178 AB.
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

Figure 10-1 SOT23-6L package outline dimension

11 Datasheet Revision History

11.1 Ver 0.1 (2026.06.16)

- Initial version Release

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